REMARKS

This is in response to the Office Action of 01 June 2004. Claims 1-20 are pending in the application, Claims 8-20 have been withdrawn, and Claims 1-7 have been rejected.

By this Response and Amendment, Claims 1-3 have been amended, withdrawn Claims 8-20 have been cancelled without prejudice or disclaimer, and new Claim 21 has been added.

No new matter has been added.

In view of the amendments above and remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to structures and methods for aligning a wafer and a reticle to each other within a stepper. The present invention relates more particularly, to the placement, structure, and compositing of alignment targets to provide for increased accuracy and/or greater manufacturing throughput. In accordance with the present invention, an alignment target is formed by at least a first exposure in a stepper, and, after moving the wafer, at least a second exposure with the wafer in the new position. The resulting alignment target now has information contained therein representing the magnitude of a stepper rotational error between the first and second exposures.

Rejections under 35 USC 102(e)

Claims 1-3 and 6-7 have been rejected under 35 USC 102(e) as being anticipated by Zhou (US Patent 6,172,409).

Claim 6 has been cancelled, thereby rendering the rejection of Claim 6 moot.

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Independent Claim 1 has been amended to more clearly that the *recited* alignment targets are located in scribe lines on opposing sides of a "first region", which, as made clear in the specification can contain one or more integrated circuits. There is no disclosure, suggestion, or motivation provided by Zhou regarding the placement of alignment targets in scribe lines on opposing sides of a stepper shot. In fact, Zhou describes a single alignment target in a single scribe line between two integrated circuits, and further describes buffer structures to surround the single alignment target to reduce or prevent contamination of that alignment target during various semiconductor manufacturing operations.

Additionally, Claim 1 has been amended to recite a property of an alignment target in accordance with the present invention, wherein a width thereof corresponds to a stepper rotational error between a first region and an adjacent second region of the wafer. Support for this amendment can be found in the specification at pages 18-25, and in Figs. 6A-6C, 7, and 8.

Claims 2-3 have been amended in a non-narrowing manner so as to make their language consistent with the amendment of Claim 1.

There is no disclosure, suggestion, or motivation in Zhou regarding the newly recited limitations of independent Claim 1. In view of the foregoing, Applicants respectfully submit that the rejection under 35 USC 102(e) of independent Claim 1, and Claims 2-3 and 7 which depend therefrom, have been overcome.

Rejections under 35 USC 103(a)

Claims 4-5 have been rejected under 35 USC 103(a) as being unpatentable over Zhou in view of Wolf, et al., ("Silicon Processing for the VLSI Era: Vol. 1" Lattice Press, Sunset Beach, CA, (1986), p. 478) and Banks ("Introduction to Microengineering", Demon Co., England (1999), p.2).

Claims 4-5 depend directly from amended independent Claim 1. As

discussed above, Claim 1 has been amended to recite a property of an alignment target in accordance with the present invention, wherein a width thereof corresponds to a stepper rotational error between a first region (i.e., a first stepper shot) and an adjacent second region (i.e., a second stepper shot) of the wafer.

Since the references do not to disclose, suggest, or provide motivation for the invention defined by Claims 4-5, which depend from amended Claim 1, Applicants respectfully submit that the rejection of these Claims under 35 USC 103(a) has been overcome.

New Claim 21

New Claim 21 is directed to a structure that provides a plurality of four-sided integrated circuit regions disposed on a wafer, separated by scribe lines; and at least one alignment target disposed in a first scribe line, the first scribe line being a common region between a first stepper shot and a second stepper shot; wherein the at least one alignment target has a width that corresponds to a stepper rotational error between the first stepper shot and the second stepper shot. Support for new Claim 21 can be found at pages 18-25 and in Figs. 6A-6C, 7, and 8.

The cited references do not appear to disclose, suggest, or provide motivation for the recited structure of independent Claim 21, wherein an alignment target is exposed a second time after the wafer has been moved within the stepper, such that the double exposed alignment target has a width that corresponds to a stepper rotational error.

Conclusion

All of the rejections in the outstanding Office Action of 02 June 2004 have been responded to, and Applicants respectfully submit that the pending Claims 1-5, 7, and 21 are now in condition for allowance.

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Appl. No. 09/737,606

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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